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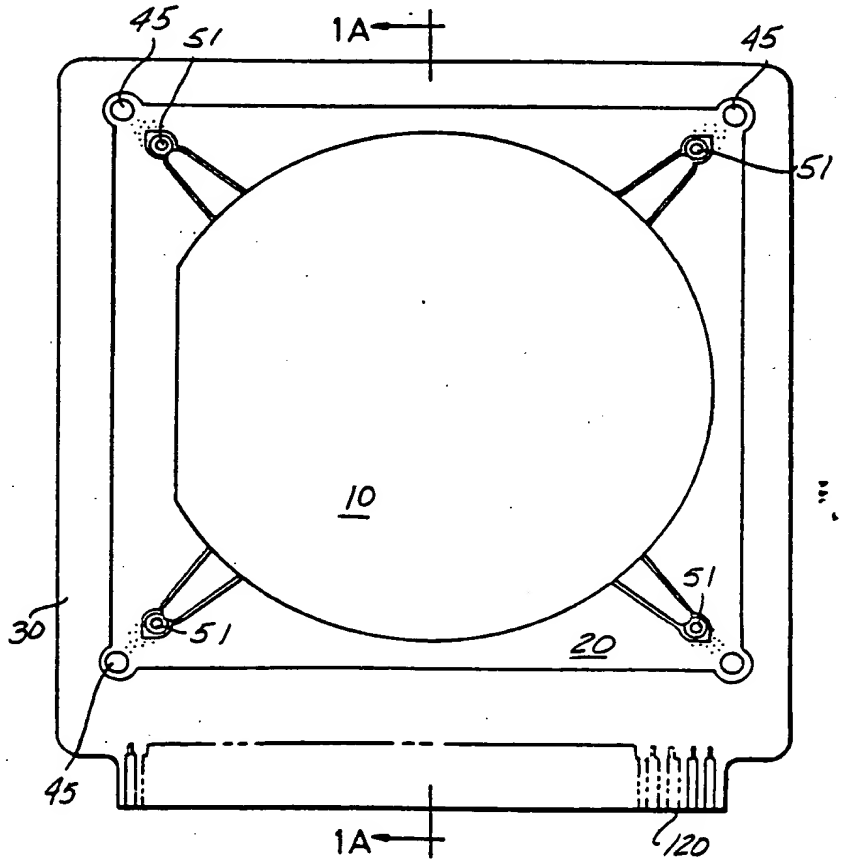
(54) Title: WAFER SCALE PACKAGE SYSTEM AND HEADER AND METHOD OF MANUFACTURE THEREOF

(57) Abstract

Wafer scale device (10, 201) on which is formed a layer of thin film as an interconnection system (203) with contact sites (202, 207) between the interconnection system (203) and die bonding sites (202) of the wafer (10, 201) to form a monolithic wafer. The interconnection system (203) has bonding sites on the surface of the wafer (10, 201) to which chips (11) are bonded to form a hybrid monolithic wafer system. The wafer (10) is packaged within a wafer package, (Fig. 4), and the packaging system utilizes a header (20) which is a flexible circuit connector between the wafer package and first level circuit board (30).



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Application number

EUROPEAN SEARCH REPORT

EP 85 90 1256

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.⁴)
X,D	WO - A - 82 02 640 (R. JOHNSON) * Page 3, line 24 - page 5, line 8; page 23, claim 1; page 24, claim 7; figure 1 * --	1,3,4	H 01 L 23/48 H 01 L 23/32 H 01 L 27/10 H 01 L 23/12
X	WO - A - 82 02 603 (R. JOHNSON) * Page 4, lines 7-22; claims 7,11; figure 1c * --	1,3,4	
X	32nd ELECTRONIC COMPONENTS CONFERENCE, May 10-12, 1982, San Diego, pages 7-16, IEEE, New York, US; Y. HSIA et al.: "A reconfigurable interconnect for in-silicon electronic assembley" * Page 8: "Empirical examination of basic concepts"; figures 3-5 * ----------	1,3,4	

TECHNICAL FIELDS SEARCHED (Int. Cl.⁴)

H 01 L 23/00
H 01 L 25/00
H 01 L 21/00

The supplementary search report has been drawn up for the claims attached hereto.

Place of search	Date of completion of the search	Examiner
The Hague	28-07-1987	DELPORTE

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
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P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
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& : member of the same patent family, corresponding document

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CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

☐ All claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for all claims.

☐ Only part of the claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid.

namely claims:

☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

X LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirement of unity of invention and relates to several inventions or groups of inventions.
namely:

1. Claims 1-4,14,15: A wafer
2. Claims 5,10-13,19: A header
3. Claims 6-9,16-18: An electronic system (a wafer scale packaging system)

☐ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.

☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid.

namely claims:

☒ None of the further search fees has been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims.

namely claims: 1-4,14,15

What is claimed is:

1. A wafer bearing interconnection lines and having an area for connection to external circuits, said area having a plurality of interconnection pads at the edge of the wafer.

2. A wafer according to Claim 1, wherein said area has a linear array of pads, with lines extending from the pads toward the center of the wafer, and wherein the wafer has additional pads between the lines extending from the pads to the interior of the wafer.

3. A wafer comprising,

a substrate bearing circuits formed thereon, and bearing an interconnection matrix which interconnects the circuits.

4. A monolithic wafer system comprising.

a combination of prefabricated circuits formed on the wafer in a prefabrication process and additional circuits bonded to the wafer to form a a hybrid system of said additional circuits and said prefabricated circuits.

5. A wafer header comprising.

a multilayer device adapted to be connected to a wafer and to an external circuit.

means on said multilayer device for providing power and ground to the wafer and from the external circuit, and means for interconnecting signal lines on the wafer to an external network, said means for interconnecting signal lines on the wafer to an external network including a plurality of bonding points on the multilayer device which are connected to lines which interconnect the bonding points to points for bonding to the external circuit.

6. An electronic system comprising

a wafer and

a header for said wafer.

7. An electronic system according to Claim 6 wherein the wafer at least one integrated circuit on the wafer which is connected to the header via an interconnection matrix on the wafer which has signal and ground points which are bonded to selected lines on the wafer.

8. An electronic system according to Claim 6 wherein the wafe carries electronic circuits formed on the wafer, which circuit are tested for interconnection of an interconnection matrix or the wafer, which in turn is connected to the header.

9. An electronic system according to Claim 8 wherein chips a downbonded on the wafer and interconnected to the matrix and coupled to said circuits and said header.

10. A header comprising.

a flexible insulating support frame.

a first metal layer affixed to a first side of said support frame having a center aperture therein.

a second metal layer affixed to a second side of said support frame.

each of said metal layers being patterned to a particular conductive pattern.

said first metal layers having a particular conductive pattern which disposes adjacent said center aperture bonding sites connected to a plurality of signal lines, and power areas and ground areas, said signal lines being formed so as to pass to the outer edges of said frame where bonds to an external circuit pattern can be made.

11. A header according to Claim 10 wherein each corner area of said frame has a flexure aperture permitting a linear distribution of strain along the center of said frame.

12. A header according to Claim 10 wherein said second metal layer has a large area ground pattern area and at least one power connection pattern.

13. A header according to Claim 10 in combination with a support printed circuit having a circuit pattern board to which said signal lines of the header outer edge are connected, and an integrated circuit device to which the said signal lines are connected at the inner edge of the header.

14. A wafer according to Claim 2 wherein said array of pads include primary pads and auxiliary bonding pads, test pads and probe points.

15. A wafer according to Claim 1 having a plurality of active die formed thereon in the form of isolated die, said die having test and bonding die contact sites, and wherein said interconnection pads are coupled to coupling sites of an interconnection system deposited on the wafer for coupling to said die contact sites.

16. A wafer scale packaging system including.

a support substrate circuit board.

a wafer scale circuit package having integrated circuits therein.

a flexible header which interconnects said wafer scale circuit package with said circuit board which may expand and contract in response to temperature changes to compensate for differential temperature expansion of said circuit board and wafer scale circuit package.

17. A wafer scale packaging system substantially as described.

18. A wafer scale package for the wafer according to Claim 1 wherein said package includes a side and top covering under which a header to said system extends, which encloses the active wafer surface.

19. A method of manufacture of a header comprising,

etching metal surfaces of a metal clad flexible insulator substrate to form a first patterned metal layer having signal lines, ground and power areas on a first metal side of said substrate and a second patterned metal layer having power and ground areas on a second metal side of said substrate.

WAFER SCALE PACKAGE SYSTEM AND HEADER AND METHOD OF MANUFACTURE THEREOF

RELATED APPLICATIONS

This application is a continuation in part of U.S. Serial No. 532391 filed September 15, 1983, entitled Wafer.

BACKGROUND OF THE INVENTION

This invention relates to a Wafer Scale Package System and Header and Method of Manufacture Thereof. The "chip", which is a basis of many of today's computer and electronic devices, an important application will be replaced by wafer scale devices. A wafer cannot perform this intended function without connection to the outside world. A wafer scale device of the type disclosed in

U.S. Serial No. 225581 filed January 16, 1981 now abandoned and continued as U.S. Serial No. 445156 filed November 29, 1982, entitled Universal Interconnection Substrate, Stopper et al, is a kind of wafer scale device to which the present application is directed. In the past, devices similar to that described in the application entitled "Universal Interconnection Substrate" were mounted in a printed circuit board and directly connected to the circuit board in the manner shown in Business Week, September 26, 1983, page 148-D. The state of the art today however generally is to the effect that small "chips" are packaged in a chip package which has within the ceramic or plastic packaging spider-like leads which lead to pins external of the package which are pressed into a connector on a printed circuit board.

A driving force between wafer force integration is that when interconnecting substrates are packaged as wafer scale devices the circuit density of the integrated circuits is increased and the distance between logic and between logic and memory become closer increasing reliability and speed. However, mechanical connection between wafers and circuit boards has to be improved in order to take advantage of increasing reliability and

speed. The wafer scale devices must be connected to the outside world.

SUMMARY OF THE INVENTION

In contrast to this present state of the art, we have been working on a new level of technology, which we call wafer scale integration. This technology utilizes the entire wafer to make a system package, as opposed to a chip package. To understand the technology, gates, diodes, resistors and other well known electrical elements are fundamental units of a circuit, and a circuit in turn is a sub-element of a die, and the die or "chip" is a sub-element of a wafer. The wafer itself, in a version of our monolithic wafer, is composed of a plurality of circuits and is capable of being an entire system. This system is of a scale much greater than the systems made on single chips for the first time approximately a decade ago. Chips during the last decade have been made which have an on board memory, an instruction processor and interconnection bus to the outside world.

By utilizing available VLSI technology and our

wafer scale integration techniques we can reduce a room size mainframe computer to a single monolithic wafer. The dicing techniques can be eliminated. In addition, we have devised methods and techniques to combine circuits which are not made on a single wafer into a single unitized wafer.

These devices are not merely improvements to the state of the art, but raise much of the technology to a new level. In order to connect the wafer scale device to the outside world we have discovered and invented how the device can be employed in wide ranging temperature applications. The wafer itself is a thin, fragile, but large area sheet. We have developed a wafer package, and a device for mounting this package to a first level connector circuit which is in the form of a printed circuit board. This package mounting device we call a header. It is a flexible circuit which incorporates the circuit technology needed to support the wafer function, is mated with certain corresponding function elements of the wafer itself, and also with the support substrate board. The combined system is rugged, lightweight and useful in high as well as very low application temperature.

The particular elements which are part of our invention are described below. It should be understood that the substantial improvements, inventions and discoveries may be better understood by reference to the appended claims and the following detailed description with reference to the drawings in which:

Figures 1 and 1A are respectively a view and section of the preferred embodiment of our wafer scale package system.

Figure 2 shows an alternate embodiment of Figure 1.

Figure 3 shows the package system of Figure 1 before it is mounted on the support board.

Figure 4 shows a wafer package of Figure 3 in partial section taken along line 3-3 of Figure 3.

Figure 5 shows a section of the header.

Figure 6 shows a corner portion of the header, while Figure 6A shows a mask for Figure 6.

Figure 7 shows the same corner as Figure 6 in a view of the other side of the header in an intermediate step of manufacture.

Figure 8 shows a finished view of the corner view of Figure 7.

Figure 9 shows a top view of a wafer which may be used in the wafer scale package system.

Figure 10 is a microscopic view of the connection edge of the wafer of Figure 9.

Figure 11 shows a microscopic view like Figure 10, showing a header edge showing alternate bonding.

Figure 12 is a view like Figure 11 showing primary bonding.

Figure 13 shows a corner of the header and wafer.

Figure 14 shows a closer view of the top portion of Figure 13.

Figure 15 shows a partial side section sketch of the wafer system package of Figure 1.

Figure 16 shows a partial side section sketch of the wafer system package of Figure 2.

Figure 17 shows a mechanical schematic of

Figures 15 and 16.

Figure 18 shows a mechanical schematic of Figures 15 and 16 at a higher temperature than Figure 17.

Figure 19 is a schematic cross-section of a preferred wafer device which is part of the wafer system.

DESCRIPTION OF PREFERRED EMBODIMENTS

Referring to the drawings in greater detail, the reader should understand that we have disclosed herein, our preferred embodiment by way of example, and alternative embodiments to our inventions and discoveries. The features which are common to all embodiments have been disclosed once. Thus we will utilize a single description of these common features in this description.

The wafer 10 is shown in Figure 1. The same wafer is shown in Figure in 31 also numbered 10 showing the header 20 before it is mounted on the board carrier 30. The wafer itself is generally described with reference to Figure 9 and features of the wafer shown in

Figure 9 are shown in Figures 3, 4, 10 and 11-14. The wafer is also shown in Figure 2 which discloses our alternative packaging embodiment which is preferred in some situations instead of a preferred embodiment of Figure 1. Figure 1A shows a cross section of the preferred embodiment taken along line 1A showing how two wafers are mounted on board 30.

Turning now to Figure 2 is the example of the wafer, each wafer has a cell areas 3 on which are mounted or deposited integrated circuits 6 similar to those shown as chips 11. These chips 11 are understood to be either directly formed on the wafer or placed on the wafer and interconnected to the wafer by means of downbonding wires 12. When hybrid circuits are incorporated on a wafer with an interconnection substrate one bonds the wafer to a cell area 3 at bonding points on the interconnection wafer. Interconnecting various circuits as integrated circuits 11 on the wafer are orthogonal lines 8 and 7 representing vertical and horizontal lines acting as padlines or netlines generally referred to as net or network lines, which are formed on the wafer 10. These lines may be programmatically interconnected at point 9. These may be formed in the in-between cell areas 5 as well as under the cell areas 3 as shown in Figure 8. In

addition, cell areas 6 may be formed on the wafer itself, with or without the illustrated hybrid circuit configuration, which can be for example monolithic memory which is interconnected to another cell area 3 or 13 via the interconnection lines 7 and 8. These cell areas can also support independent hybrid integrated circuits 11 and interconnected thereto via bond wires 12.

In order to connect the generally described wafer scale integrated circuit device one embodiment of which is shown in our copending applications U.S. Serial No. 445156, previously referenced in application Section No. 360177, filed March 22, 1982 and entitled Computer Apparatus and Method of R.R., by Johnson et al. which is herein fully incorporated by reference, some means is needed to connect the wafer scale device to the outside world.

We accomplish this by the use of the wafer 10, a header 20, which in turn is connected to a printed circuit board 30 in the form of a wafer scale package system. The wafer, header and board package system is shown in Figures 1, 2 and 3 with details shown in additional figures.

As shown in Figure 1, our preferred embodiment,

the wafer is mounted backside out on the printed circuit board and connected to the header such that the integrated circuits 6 and 11 are disposed toward the printed circuit board. In the alternative preferred embodiment is shown in Figure 2, these devices are disposed on the printed circuit board 30 facing outwardly.

In both embodiments the header 20 is a substantially identical device. The cross section of the header 20 is represented generally in Figure 5. It is a flexible circuit intended to facilitate the connections from the wafer scale device to the next higher level of package and/or first wiring on the board 30 as described further herein. It provides at least 800 signal lines including 32 signal ground connections for a net of 768 signal lines as well as additional connections for power ground and power (single voltage). As shown in Figure 4 section the header is fabricated from a thin insulator 21. Preferably manufactured from Kapton or alternatively Mylar and approximately 25 microns, that's 25 um (1 mil) thickness. This insulator 21 is coated on the top with an adhesive such as Pyralux or its equivalent as adhesive 22 which is approximately also 25 microns (1 mil) thick. Similarly, on the bottom an adhesive 23, Pyralux or its

equivalent, is applied to the bottom of the insulator 21. A top conductor 24 is applied to the adhesive 22. This is preferably of copper, approximately 60 microns (2.4 mil) thick. Also preferably made of "one ounce copper". Similarly a like bottom conductor 25 is similarly affixed with adhesive 25 to the insulator 21.

The top surface is flash plated with a top surface plating 26. This top surface plating is gold, at least 1.2 micron (50 micro inches) thick, over nickel which is also at least 1.2 micron (50 micro inches) thick.

On the bottom surface 27 is similarly Flash plated a bottom surface plating 27 of gold over nickel each approximately 1.2 micron (50 micro inches) thick.

While details of the header 20 will be described in greater detail, an understanding of the manufacturing method coupled with the particular features which are important for the header 20 will be first described.

As shown in Figures 5 and 1, the top (top means the surface viewing the reader in Figure 1, and hidden from the reader in Figure 2) metal layer, which is

preferably in this orientation predominately a ground plane, is a part of the Figure 1 preferred embodiment which is mounted on the printed circuit board so as to face the reader. The bottom layer, which is the metal layer carrying signals from the inside or wafer to the outside world is not shown in Figure 1. In an alternative embodiment shown in Figure 2, the top layer is shown facing the inside or printed circuit board side of the assembly while the top layer or ground plane is hidden from view. Thus preferred embodiment in Figure 1, and the alternate preferred embodiment in Figure 2 show essentially the same header 20. The orientation of the header in the different preferred embodiments has significance which will be described below.

The signal ground layer or bottom plated layer of copper and gold of Figure 5 (which is shown in mask Figure 2B) also contains structure used in the manufacturing process of plating and drilling. These process parts are discarded when the header is trimmed to size. The signal ground plane is shown in view in Figure 2.

The first step of the manufacturing process of the header is to prepare a large sheet of material, from

which say twenty headers will be fabricated. This sheet is a lamina composed of the flexible insulator 21 and the copper layers 24 and 25 including the adhesive layers 22 and 23.

During the manufacturing process the ground layer or top layers 24 and the signal ground layers 25 are replicated to produce the multi-header mask used by the manufacturer. The insulator layer has holes drilled therethrough. Some of the structures in the signal ground masks are formed with openings 45 as seen in Figure 2B in the metal layers so as to show the location of the holes to be drilled through the insulating layer 22. The multi-header single ground mask is used to set up an automatic drilling machine using the openings which will be described. The manufacturer may add alignment marks outside the active header area for his own use so that in the manufacturing process alignment holes may be drilled in the sheet in areas which be later discarded.

As holes are drilled an electroless plating process is used to deposit copper in the holes and at least .5 mil of copper is plated on both the sheet and in the holes. A photo resist is added to both sides, and exposed using two multi-header masks. Since the openings

in the signal ground layer 25 for drill positions are smaller than the holes drilled in the material, the resist will fill the holes and protect the edges from etching. Both sides of the sheet are then etched in one step, leaving a number of header patterns all of which are temporarily connected together in a single circuit (for additional plating). The resist is then removed.

Additional copper is plated on the circuit, in part to compensate for undercutting the resist etching, and in part to increase the thickness of the metal lines and the amount of copper in the plated through holes. The next step in the plating operation adds the layer of nickel to the circuits. A flash of gold is then added immediately, to preserve the nickel surface. Since gold is so expensive, the ground side 24 is masked to prevent further plating. Additional gold is then plated, to provide a good surface for wire bonding. Then the plating mask for the signal ground side 24 is then removed. Then individual headers are cut from the initial sheet, using either a steel rule die or hard tooling. The initial alignment holes which will be described are also used in this punching operation.

Figure 6 shows the signal ground layer of the

header before it is trimmed. When it is trimmed it follows the drawing shown in Figures 1, 2, 3, and 6. Figure 6A also shows a mask of the signal ground layer of the header 20 before it is trimmed which shows in more detail but in negative form the linear side of header 20.

Generally as shown in Figure 6A, the header has a group of signal and ground lines which are adapted to be connected to the wafer itself and which run to the outside world. Each side of the header has 200 signal lines including 8 signal ground connections. The signal lines run directly from inside of the header in parallel and at some point on a V-shaped spreadline 39. The direct connect inside signal lines 36 turn at an angle of approximately 120 degrees and continue toward an outside connecting area 37. The angular lines 38 then turn at the same angle and connect to bonding pads in the area 37. The width of the bonding pads in the area 37 differ. Lines which act as signal ground lines 42 are wider at the outside bonding point, so as to permit a via hole 55 through to the ground plane (the top surface shown in Figure 5) as shown in Figure 3 and 8. The other bonding pads 41 which in Figure 6 are approximately twice the width of the signal lines shown as 38 and 36.

The header is fabricated preferably as a generally rectangular or square shaped final device having alignment holes 33, not through plated, punched in each of the four corners. Each of the four corners has a pattern formed thereon which is substantially identical at each corner. The alignment holes 33 that are not through plated are punched out as shown in Figures 3 , 1 and 2. These alignment holes are used to position the header itself in position for soldering onto the printed circuit board 30. At each corner are also four through plated holes 51 which are used for power hook-up, and four corner cut-outs 47, to be considered corner apertures. The purpose of them will be described in greater detail hereinafter. The corner alignment holes 33 are used for alignment, mounting and for ground hook-up. The plated through holes 51 are used for power hook-up to the bottom area 34 and the four corner flexure apertures or cut-outs 47 are utilized for obtaining linear movement of the sides of the header after attachment to board 30 as well as, also importantly, to enable grasping of the header by a holding fixture during subsequent manufacture. The four V-shaped corner cut-outs 47 have a wider section aperture nearer to the center square donut-hole area of the header and are

narrower across the edge adjacent the corners. This permits the edge of the wafer 10 to be gripped directly by a fixture in a subsequent manufacturing operation. The wafer can be seen in Figure 2 from the bottom side and the wafer can be seen in Figure 1 from the top side. The round plated through holes 51 and the four corner cut-outs need not be but can be plated through. In addition the header contains 138 small via holes which are used exclusively for electrical connections between the top and bottom metal layers. The drill diameter of these holes is approximately 0.5 micrometers or 0.018 inches before plating. The holes are plated through and it doesn't matter whether or not the holes are closed by the plating process. Locations of these via holes are marked by holes drill size in the mask to be used for the patterning of the metal layer.

Each side of the header along the outer edge has 8 via holes 55 in Figures 6 and 8 through the signal ground lead 42 on the bottom of the header which connects through to the top ground plane of the header. Again, the top and bottom in the Figures 1 and 2 may be thought of as being reversed. The primary consideration is that the ground plane is the metal conductor which is shown in detail in Figure 8. Figure 7 is a detail formed prior to

the use of the blanking die, being representative of an intermediary step in the manufacturing process prior to Figure 8. In Figure 8 there is shown one corner of the wafer in greater detail which shows a number of via holes. Included therein are, on each side, two of the 8 via holes 55 along the outside edge of the header which connects the center signal ground line of a group of 25 lines to the ground plane which is the top of the header in Figure 1. The center lines or signal ground lines do not have a common ground connection at the inner edges of the header. Instead of a ground connection area 49 at the inner edge of the header is each provided with a total of 8 via holes 57 is provided for each of the sides of the four fields with 200 lines each.

Thus, as shown in Figure 6, at each corner are located 8 inner corner via holes 57 which connect the power ground bonding area of the back of the header which has the main pattern to the ground plane top of the header seen in Figure 8. Also at each corner of the signal lines are inner ground via holes 56 which connect to the ground.

In addition, at each of the outer corner areas of the header there are 14 external power ground hook-up

area — via holes 58 connect the external power ground hook-up area 59 to the top ground plane (Figures 6 and 8).

Adjacent the V-shaped corner cut-out on the top side is a round solder splash area separated from the ground plating by a circular area of insulator. The purpose of this is to prevent solder splash from the voltage hole 51 utilized for power hook-up so that it does not connect to ground.

Turning now to Figure 2, the circled section of Figure 2 is shown in more detail in Figure 4. The Figure 2 section shown in Figure 4 will be described in greater detail. It will be appreciated that Figure 2 is a view which shows the lid of the package removed. Thus in Figure 4 the underlying printed circuit wafer package support and interconnect board is shown as bearing an encapsulated wafer 10 of the hybrid type. This encapsulated wafer bears chips 11 which are downbonded to the wafer 10. The printed circuit board 30 is not shown in full detail in Figure 12. The header 20 is physically attached to the wafer 10 and adhesively attached to the header is a package side wall 101 to which a lid 105 is attached by a lid adhesive 103. Chips 11 are adhered to

the wafer 10 adhesively. The bonding points on each chip are connected to a bonding point on the wafer 10 via bond wire 104 and another lead from the wafer 10 is connected to a signal lead 102 by another bond wire. The entire device is potted by a polymer encapsulant 106 and the lid adhesively attached.

In Figure 2 the wafer is shown with its face up. Alternatively and as preferred as shown in Figure 1, the wafer has the ground plane of the header up and the patterned signal ground side down, for connection of the lines on the header to the outside world. These may be connected either directly to another port, signal line, or another wafer by a bus structure. This may be inserted into a slot bus fixture to form a main frame. Which of the slot connectors 120 are connect to which bonding pads on the header is a matter of specific adaption to a purpose required of the device.

Each wafer has a connection rim of a wafer 10 as shown in Figure 9. The rim structure area 74 is shown in part in an enlarged size view Figure 10 and also shown in details in Figures 11 and 14. In Figure 10 is shown a design portion of the rim 74 of Figure 9 in which 61 is a primary bonding pad and 62 is a secondary bonding pad

which is used for an alternate bonding site in the event there is something wrong with the intended netline 7 or 8 attachment at the primary pad 61 and it is needed to have an external signal at that particular point on the header. We have additionally provided two test points 63 and 64 in the wafer connection rim for determining how an anti-fuse is programmed. The area of the rim functions as test points to validate the wafer before we proceed any further after fabrication. Probe or bonding points 65 and 66 are additional probe points to check the continuity of the netline 7 or 8 segments, so that one can get on one end, for example at a primary pad 61, and test whether that point can be connected on one other side of the wafer at a probe point 65 on that other side of the wafer. By probing the two points we can verify that the line segment 7 or 8 extending from pad 61 on one side to a test pad 65 on the other is in fact connected with no openings. Figures 11 and 14 show bonding at various points at the edge of the wafer to the header. As seen in Figure 13 a corner which has a ground bonding area 49 to the ground plane and a voltage bond site 34 both of which use a plurality of voltage and ground bond wires 130 and 131. Figure 12 shows the number of signal bond wires going from the primary pads directly over to

the cross-bonding position 36 on the header. Figure 11 also shows an alternate bond wire 134 connecting from a secondary pad 67 to the corresponding position 36 on the header. This is the connection that is used in the event that there is a problem with the netline 7 associated with the primary bonding pad site. We can go to an alternate one to pick up an adjacent redundant netline 137.

The Figure 14 shows how multiple connections need to be made from the ground point (like the voltage connect point) on the rim 74 from the power point 99 on the rim 44 to the voltage portion 34 on the header. Similarly, the multiple bonds would be made from a similar ground point connection on the rim to the ground point 49 on the patterned surface of the wafer which is connected then to the ground top of the header by way of the via holes 57 as shown in the sketch Figure 13 and Figures 8 and 6.

Figure 15 is a schematic representation of the mounting of a wafer on a printed circuit board in accordance with Figure 1 while Figure 16 is a similar schematic showing the mounting of the wafer device on a printed circuit board in accordance with Figure 2.

— Figure 18 is a schematic mechanical view of the wafers of Figures 14 and 15 at the time the wafer is mounted on the printed circuit board or at the period of high-temperature operation.

Figure 17 is a view of the printed circuit board of Figures 14 and 15 when the wafer is in operation in a cooler environment.

Referring now to Figure 18, the header 20 is mounted on the printed circuit board 30 with the wafer 10 in place. Essentially the header and wafer are at the time of mounting in the form as shown in Figure 3. Preferably the header is bonded to the printed circuit board at a high temperature so that the header is elongated between printed circuit board bonding point 161 and wafer bonding point 162. Thus, the header leads are made to contact corresponding leads 20 of the printed circuit board. In this manner, the lines from the wafer 10 exit through the header 20 to the leads 120 on the printed circuit board. There they are connected to the outside world. Mechanically, there may be some thermal difference in the coefficient of expansion between the wafer 10 and the printed circuit board 30. The use of the flexible header allows the connection to compensate for

changes in temperature. When the circuit board normally has a slightly higher coefficient of expansion than the wafer assembly 10 and a mechanical representation of this high temperature is shown in Figure 18, that is at a temperature of say approximately between 150 and 200 degrees or even higher as at a solder temperature below temperature which will affect the wafer package but higher than the normal maximum storage temperature say 100 degrees. When this board cools it contracts and lifts the wafer slightly from the printed circuit board as shown in Figure 17. Thus, pivot points 162 and 161 enable the header to compensate for varying temperatures in operation of the device. The flexible aperture 47 at each corner of the wafer allows for the expansion and contraction and permits a square or linear lift on each side of the wafer package.

Figure 19, is a single drawing illustrating the preferred wafer embodiment of our invention as disclosed in U.S. Serial No. 532391.

The details of Figure 19 can be understood by those skilled in the art who know that a wafer is usually a very thin cylinder of silicon on which die are deposited. Figure 19 represents a cross section of that

silicon wafer and of the other items we use and which we shall describe.

In U.S. application Serial No. 225581 continued as U.S. Serial No. 445156 incorporated herein by reference, there was disclosed a wafer substrate for integrated circuits which by itself may be made either of conductive or non-conductive material. This substrate, in the present invention, references the base monolithic wafer. This substrate for net and pad lines carries two planes or layers of patterned metal, thus providing two layers of interconnection. This patterned metal is considered to be an interconnection system within the meaning of this application. In the prior application, as now known from that application, the metal layers can have connections which are formed by amorphous semiconductor material. This, is by way of an amorphous via, as described therein. Connections between the metal layers or between the metal layers and the substrate can be made through via holes in the insulation layer between metals or between layers respectively. In this prior application, and in the presently described embodiment, the real estate of the wafer is divided into special areas called cells and signal hookup areas and power hookup areas are provided. In the prior

application, it was disclosed that the cells were intended to host integrated circuit chips in a hybrid system of chips and metal layers with the interconnections providing signal connections between the chips on the surface.

Unlike the prior application, this embodiment utilizes a different substrate. The preferred substrate has been replaced by a silicon wafer 201 (corresponding to 10) with active die incorporated on it, which die are isolated one from the other, and which each have die contact sites 202 normally used for probing during testing and for bonding during packaging. To the wafer 201, and on the upper die carrying surface, has been layered a thin adhesive layer of polyimide resin insulation layer 204. This resin, during the process of manufacturing the monolithic wafer, is cured and then etched to provide holes through the surface of the wafer to the die contact sites 202 so that these are covered temporarily. The resin performs the principal task of smoothing the surface of the wafer, which is important to subsequent processing and improves step coverage. Thereafter during the process of manufacture of the monolithic wafer a thin film interconnection system 203, of which the prior interconnection system which has been

incorporated by reference as a preferred example, is deposited on the insulation layer 204.

The interconnection system 203 has incorporated therein its own contact sites. On the upper surface are bond contact sites 205, situated at sites suitable for wire bonding. There are probe contact sites 206 suitable for probing with a test probe 215, and there are coupling contact sites 207 suitable for coupling of the interconnection system to the underlying die at die contact site 202. While in general any contact site may be coupled to any contact site, there is a special direct connection 208 between the probe contact sites 206 and the coupling contact sites 207 for the purpose of making direct test access to the buried contact site of 207 and coupled die contact site 202.

One should note here that wafers with isolated die formed thereon are common techniques in the intermediate process of making circuits. The wafer of the preferred embodiment is made like these wafers. The interconnection system which has been described, is programmable in the manner taught by the aforementioned prior application so that interconnection can be made for signal purposes throughout any or all of the dies on the

wafer, which previously had been isolated. The underlying die can be a plurality of 64K or 256KRAM die, and these can be unified into a mass memory.

These die can be unified into a full system, which can include instruction processor chips, I/O interfaces, and many other chips which are required to make a full system. The die can be replaced, if not in working order or unwanted, by a substitute die. The additional chips used to make a full system or the substitute die can be placed over the die on the wafer by adhesively bonding the downbond hybrid chips 207 carrying the desired circuits where they are placed on the surface on the interconnection system 203. Then a wire bond 211 is made to selected bonding sites, as from a site on the chip 209 to an upper bond contact site 205. Similarly, an upper bond contact site 205 can be used to bond an external wire bond 212 to a printed circuit board 210 but preferably to a header 20. Stitch bonds 213 may be made between upper bonding sites 205 of the wafer. All of the interconnections of the system make the wafer into a true monolithic wafer, and when additional or substitute chips are downbonded to the surface of the wafer we consider this a hybrid monolithic wafer system. This wafer system is preferably packaged in the system employing the

previously described header.

The inventions and discoveries claimed herein have been described in various examples. The combinations claimed include the specific examples, and combinations of specific examples and combinations of parts of the specific examples. After a review of this description, those skilled in the art, both now and in the future, will envision modifications and alterations which may be equivalent of the inventions and improvements and their combinations claimed. Such modifications should be deemed to be within the scope of the claims when utilizing the inventive nature of our inventions. This is a new technology, and it is believed this disclosure extends beyond what was possible before our disclosure.

What is claimed is:

1. A wafer bearing interconnection lines and having an area for connection to external circuits, said area having a plurality of interconnection pads at the edge of the wafer.

2. A wafer according to Claim 1, wherein said area has a linear array of pads, with lines extending from the pads toward the center of the wafer, and wherein the wafer has additional pads between the lines extending from the pads to the interior of the wafer.

3. A wafer comprising,

a substrate bearing circuits formed thereon, and bearing an interconnection matrix which interconnects the circuits.

4. A monolithic wafer system comprising.

a combination of prefabricated circuits formed on the wafer in a prefabrication process and additional circuits bonded to the wafer to form a a hybrid system of said additional circuits and said prefabricated circuits.

5. A wafer header comprising.

a multilayer device adapted to be connected to a wafer and to an external circuit.

means on said multilayer device for providing power and ground to the wafer and from the external circuit, and means for interconnecting signal lines on the wafer to an external network, said means for interconnecting signal lines on the wafer to an external network including a plurality of bonding points on the multilayer device which are connected to lines which interconnect the bonding points to points for bonding to the external circuit.

6. An electronic system comprising

a wafer and

a header for said wafer.

7. An electronic system according to Claim 6 wherein the wafer at least one integrated circuit on the wafer which is connected to the header via an interconnection matrix on the wafer which has signal and ground points which are bonded to selected lines on the wafer.

8. An electronic system according to Claim 6 wherein the wafer carries electronic circuits formed on the wafer, which circuits are tested for interconnection of an interconnection matrix on the wafer, which in turn is connected to the header.

9. An electronic system according to Claim 8 wherein chips are downbonded on the wafer and interconnected to the matrix and are coupled to said circuits and said header.

10. A header comprising.

a flexible insulating support frame.

a first metal layer affixed to a first side of said support frame having a center aperture therein.

a second metal layer affixed to a second side of said support frame.

each of said metal layers being patterned to a particular conductive pattern.

said first metal layers having a particular conductive pattern which disposes adjacent said center aperture bonding sites connected to a plurality of signal lines, and power areas and ground areas, said signal lines being formed so as to pass to the outer edges of said frame where bonds to an external circuit pattern can be made.

11. A header according to Claim 10 wherein each corner area of said frame has a flexure aperture permitting a linear distribution of strain along the center of said frame.

12. A header according to Claim 10 wherein said second metal layer has a large area ground pattern area and at least one power connection pattern.

13. A header according to Claim 10 in combination with a support printed circuit having a circuit pattern board to which said signal lines of the header outer edge are connected, and an integrated circuit device to which the said signal lines are connected at the inner edge of the header.

14. A wafer according to Claim 2 wherein said array of pads include primary pads and auxiliary bonding pads, test pads and probe points.

15. A wafer according to Claim 1 having a plurality of active die formed thereon in the form of isolated die, said die having test and bonding die contact sites, and wherein said interconnection pads are coupled to coupling sites of an interconnection system deposited on the wafer for coupling to said die contact sites.

16. A wafer scale packaging system including.

a support substrate circuit board.

a wafer scale circuit package having integrated circuits therein.

a flexible header which interconnects said wafer scale circuit package with said circuit board which may expand and contract in response to temperature changes to compensate for differential temperature expansion of said circuit board and wafer scale circuit package.

17. A wafer scale packaging system substantially as described.

18. A wafer scale package for the wafer according to Claim 1 wherein said package includes a side and top covering under which a header to said system extends, which encloses the active wafer surface.

19. A method of manufacture of a header comprising.

etching metal surfaces of a metal clad flexible insulator substrate to form a first patterned metal layer having signal lines, ground and power areas on a first metal side of said substrate and a second patterned metal layer having power and ground areas on a second metal side of said substrate.

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No [18]
Y	US, A, 3,983,479, PUBLISHED 28 SEPTEMBER 1976, LEE ET AL	1-19
Y	US, A, 3,781,683, PUBLISHED 25 DECEMBER 1973, FREED	1-19
Y	IBM TECHNICAL DISCLOSURE BULLETIN, VOL. 15 NO. 2, ISSUED JULY 1972, BODENDORF ET AL, "ACTIVE SILICON CHIP CARRIER," PAGES 656-657	1-19
Y	IBM TECHNICAL DISCLOSURE BULLETIN, VOL. 19, NO. 3, ISSUED AUGUST 1976, HALLAS ET AL, "TEST STRUCTURE FOR SEMICONDUCTOR CHIPS", PAGES 898-899	1-19
Y	IBM TECHNICAL DISCLOSURE BULLETIN, VOL. 17, NO. 9, ISSUED FEBRUARY 1975, GHATALIA ET AL, "SEMICONDUCTOR PROCESS DEFECT MONITOR", PAGES 2577-2578	1-19
Y,E	IBM TECHNICAL DISCLOSURE BULLETIN, VOL, 27, NO. 10a, ISSUED MARCH 1985, "PLUGGABLE-MODULE POWER-CONNECTION MECHANISM", PAGES 5599-5600	1-19

INTERNATIONAL SEARCH REPORT

International Application No PCT/US85/00280

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

INT. CL.[3] H01L 23/48, 23/32, 27/10, 23/12
U.S. CL. 357/45,75, 80, 68, 71; 324/51, 73R

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
US	357/45, 75, 80, 68, 71 324/51, 73R

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
A	US,A, 3657805, Published 25 April 1972, Johnson	6-9
P,X	US,A, 4484215, Published 20 November 1984, PAPPAS	1-19
Y	US,A, 4220917, Published 02 September 1980, McMahon Jr.	1-19
Y	US,A, 4257061, Published 17 March 1981, Chapel, Jr. et al	1-19
A	US,A, 4246595, Published 20 January 1981, Noyori et al	1-19
Y	US,A, 4074342, Published 14 February 1978, Honn et al	1-19
Y	US,A, 4021838, Published 03 May 1977, Warwick	1-19

* Special categories of cited documents: [15]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
06 MAY 1985	20 MAY 1985
International Searching Authority [1]	**Signature of Authorized Officer [20]**
ISA/US	Andrew J. James

Form PCT/ISA/210 (second sheet) (October 1981)

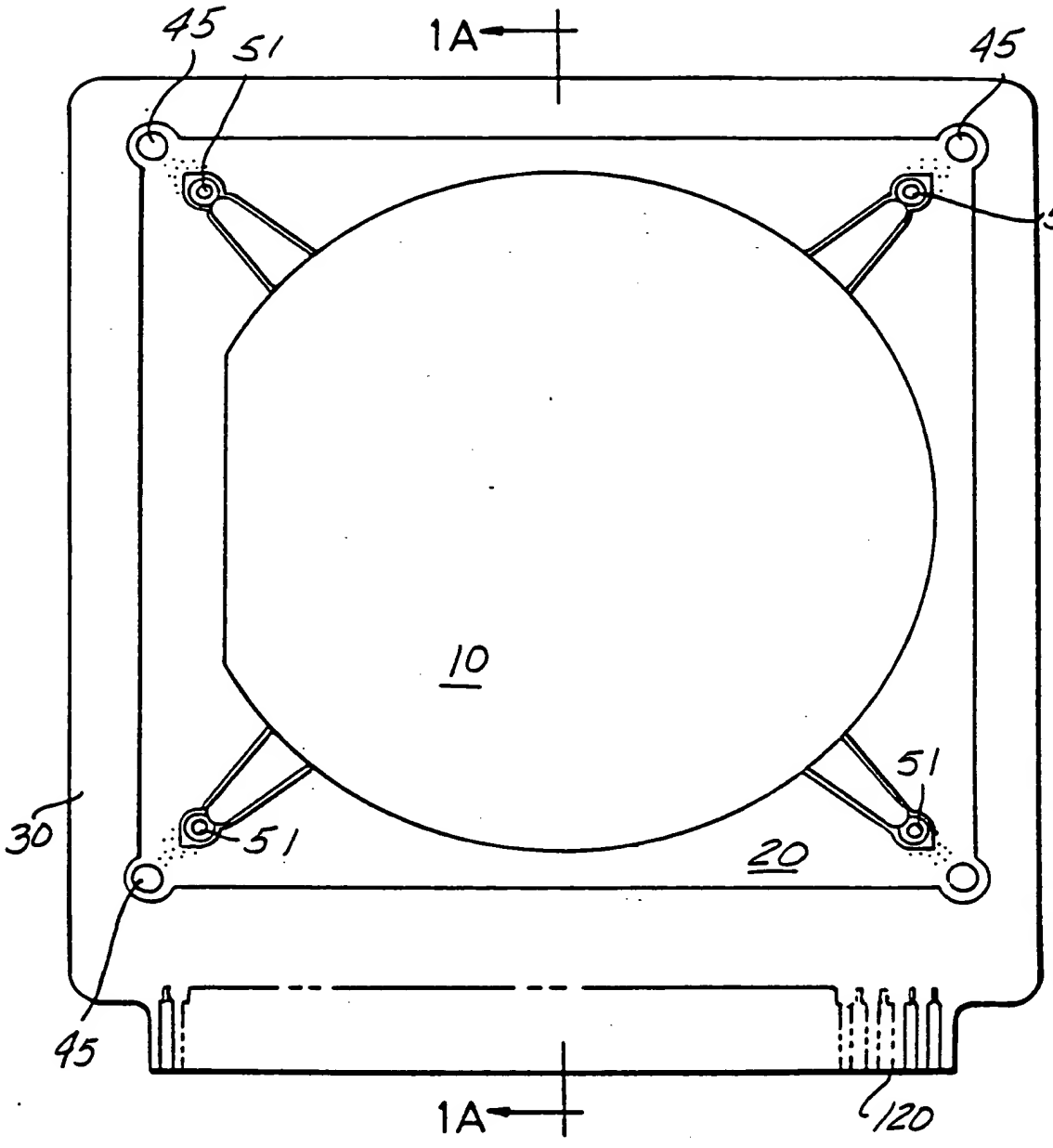

FIG-1

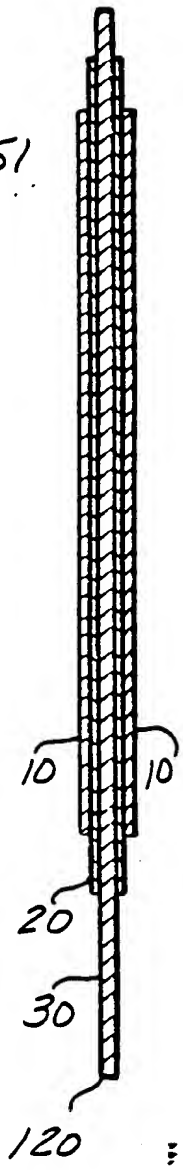

FIG-1A

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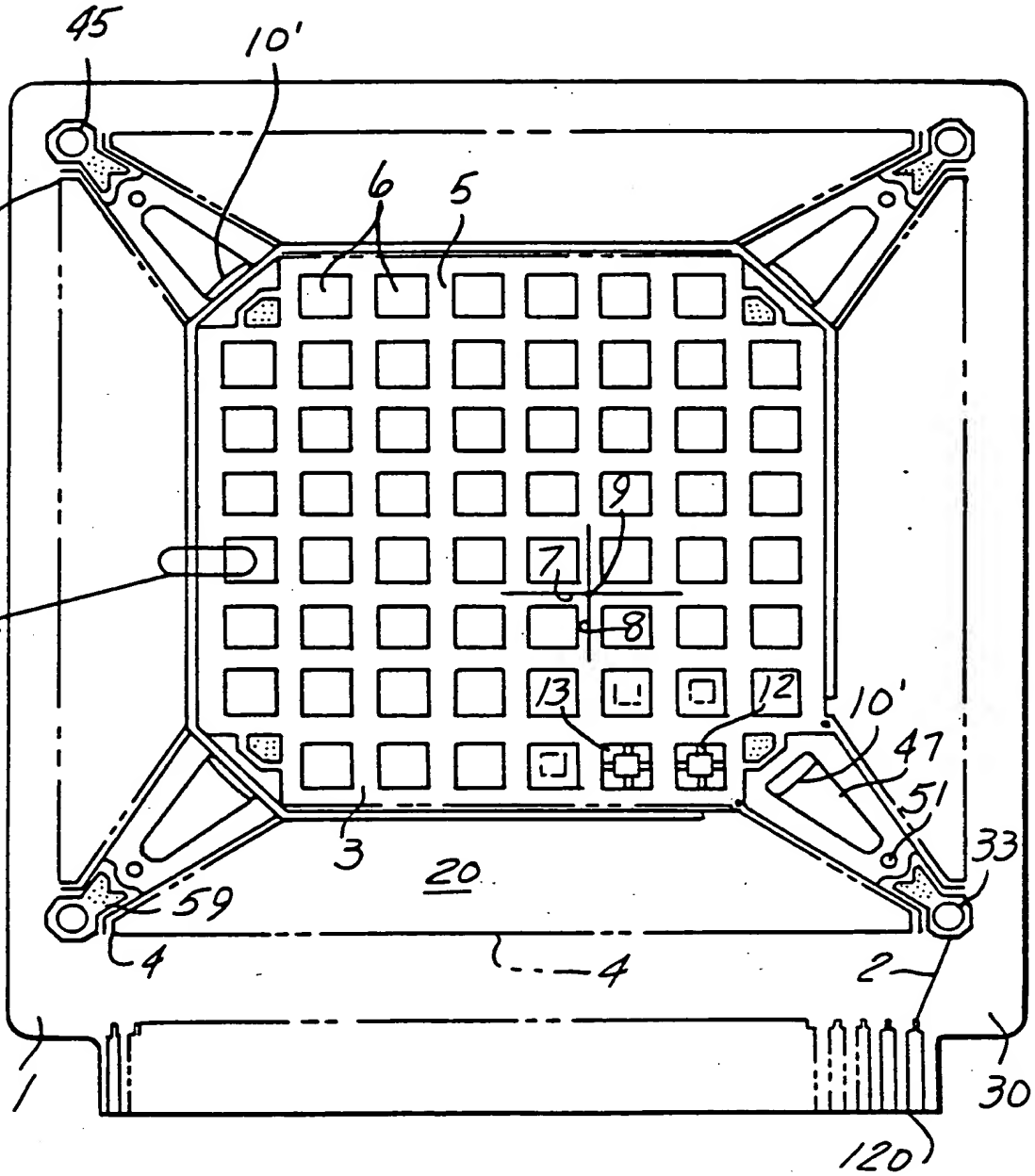

FIG-12

FIG-2

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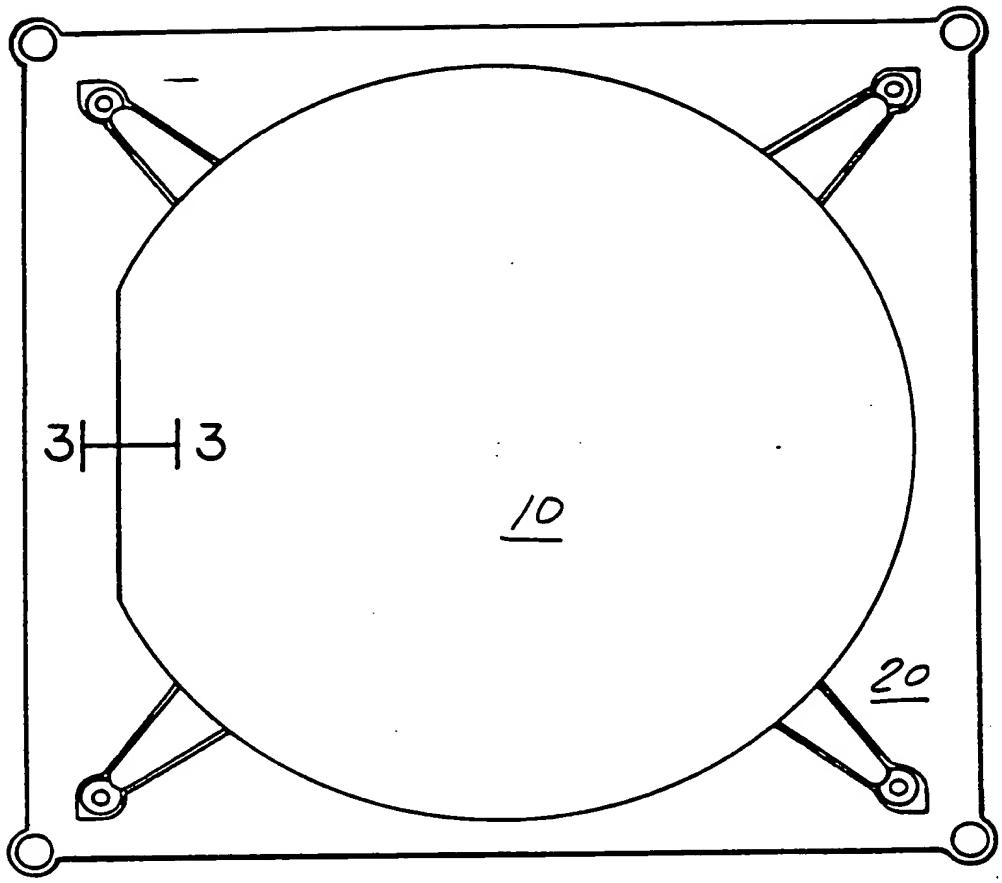

FIG-3

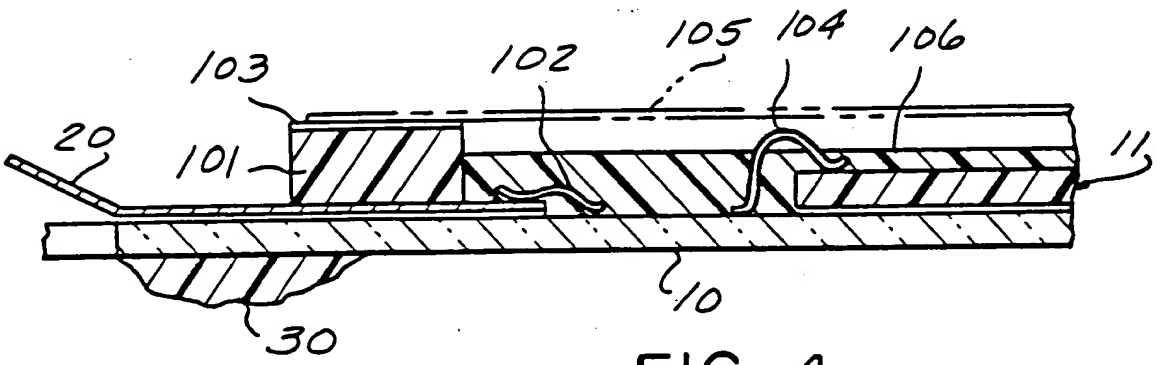

FIG-4

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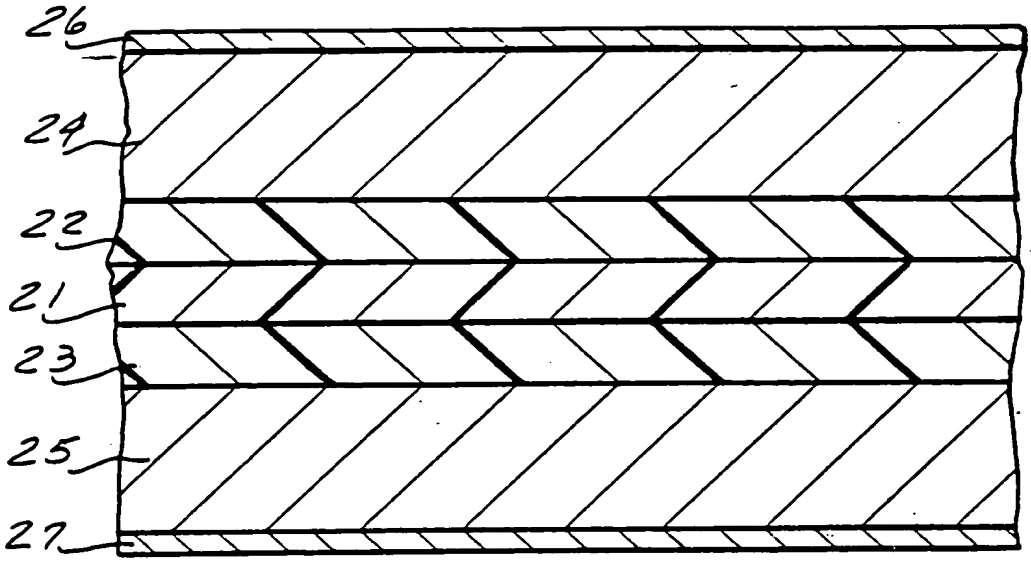

FIG-5

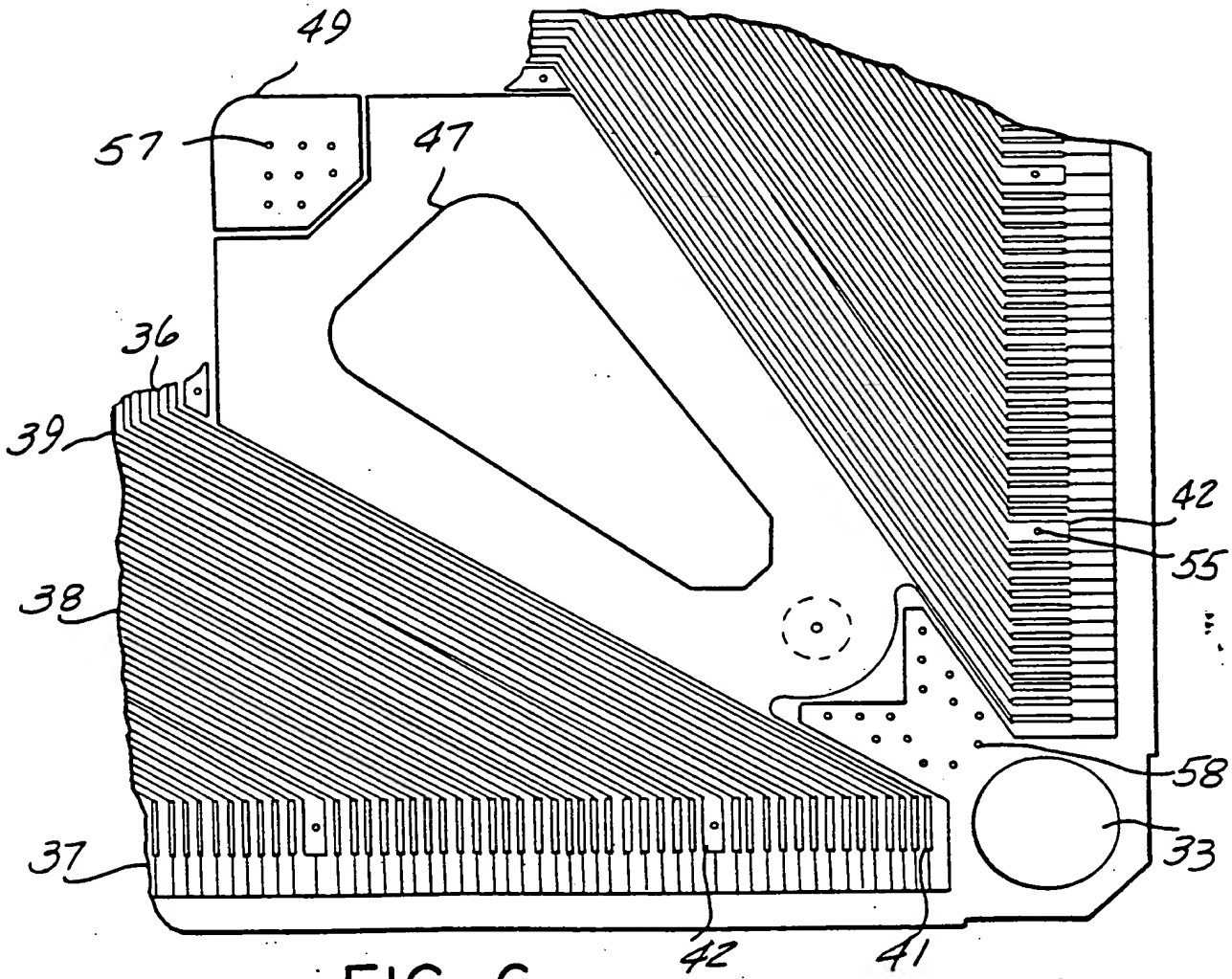

FIG-6

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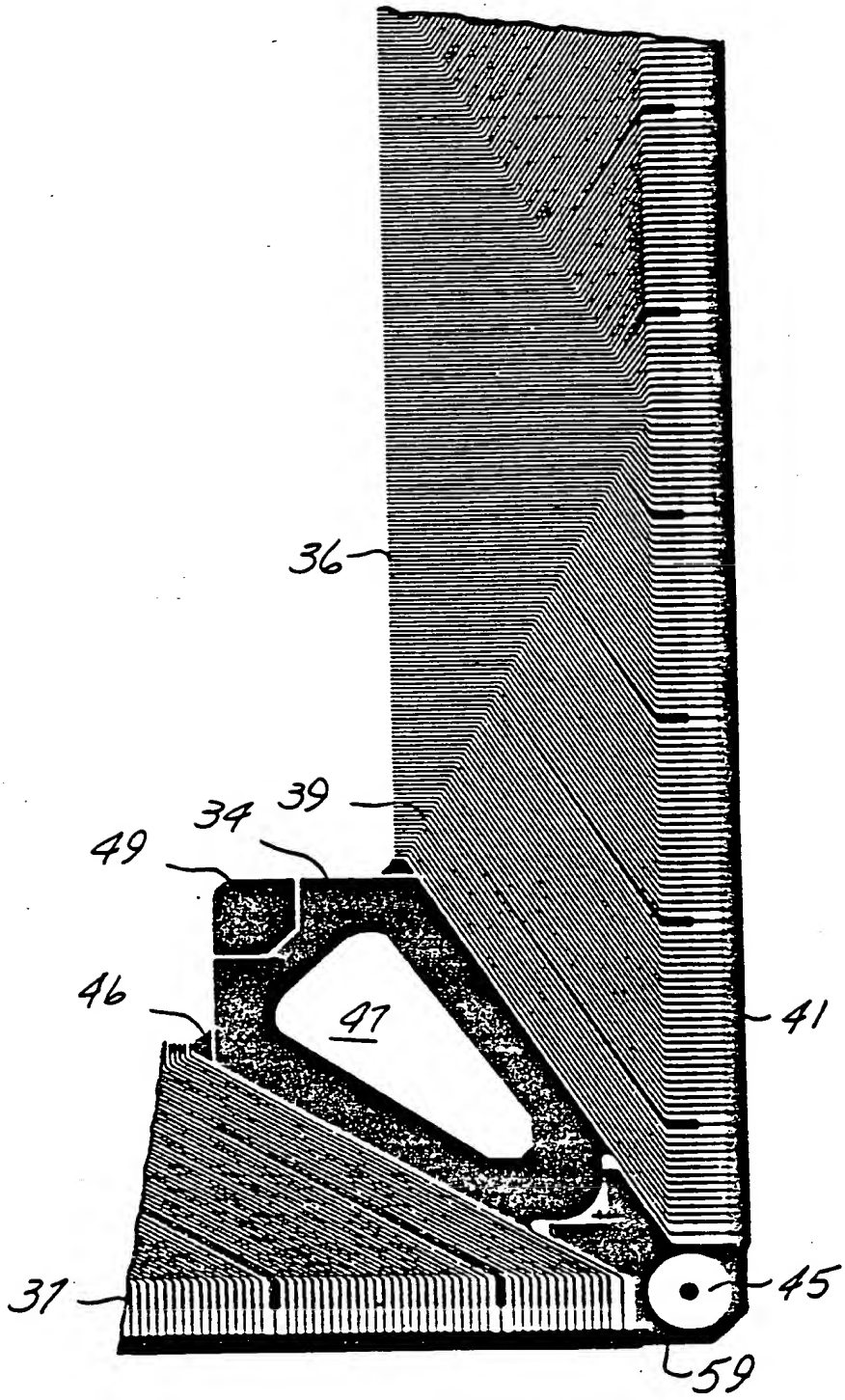

FIG-6A

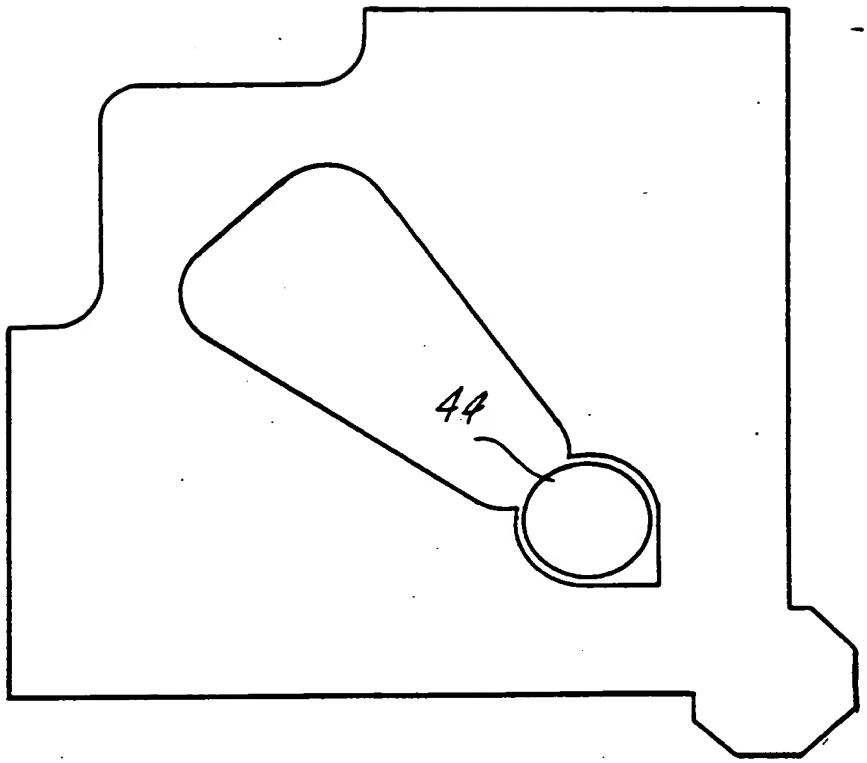

FIG - 7

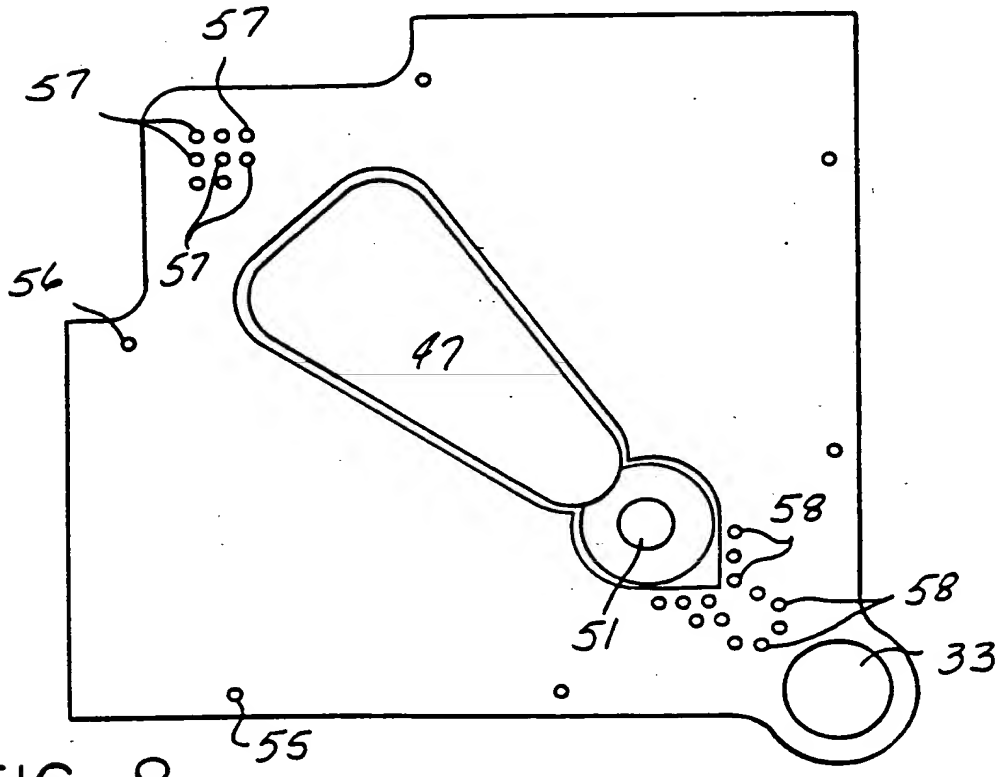

FIG - 8

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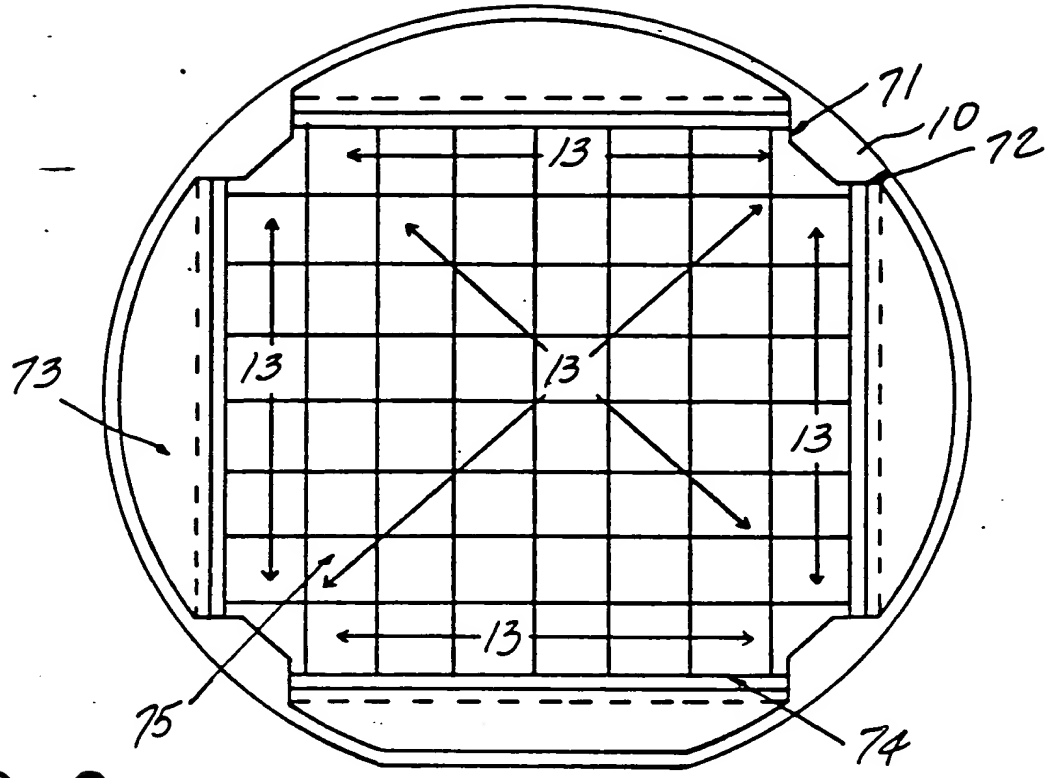

FIG-9

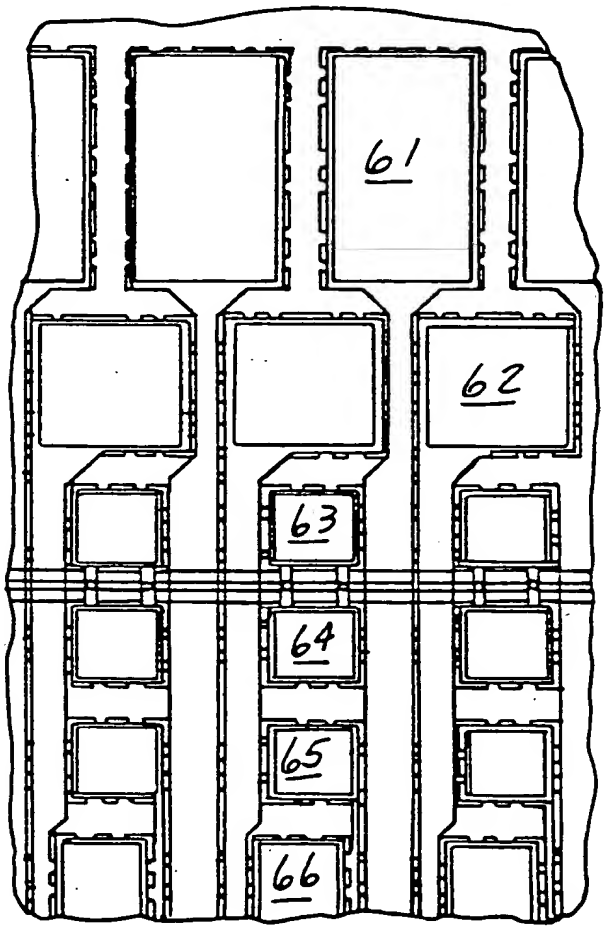

FIG-10

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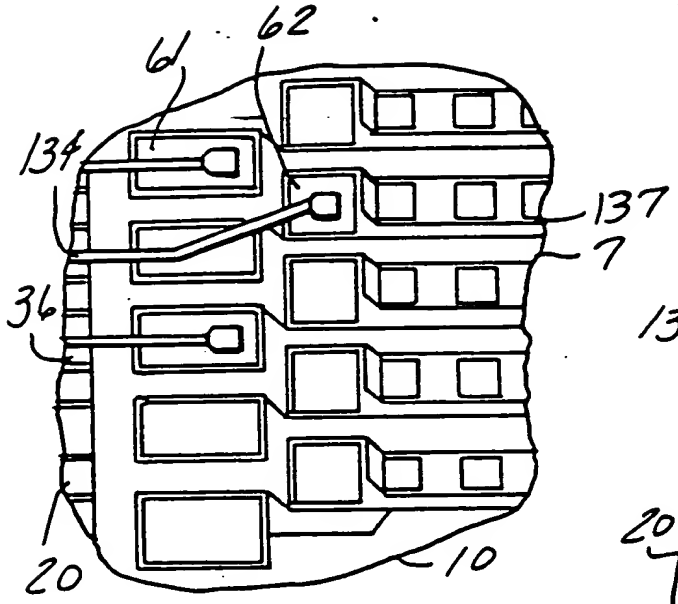

FIG-11

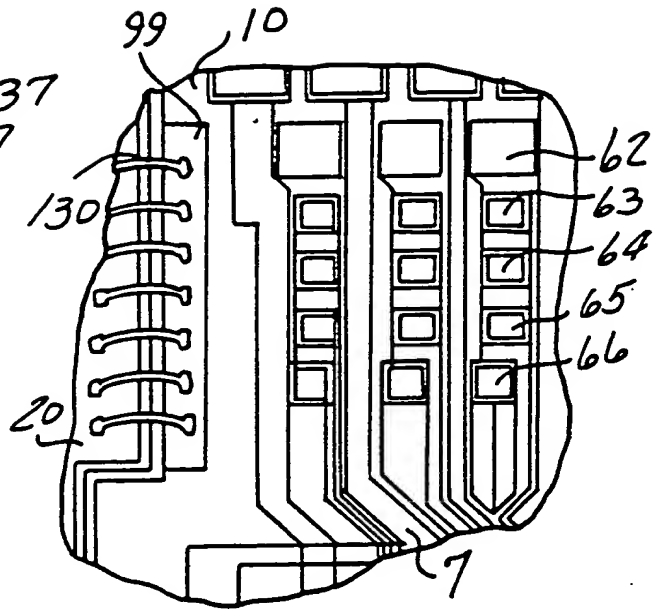

FIG-14

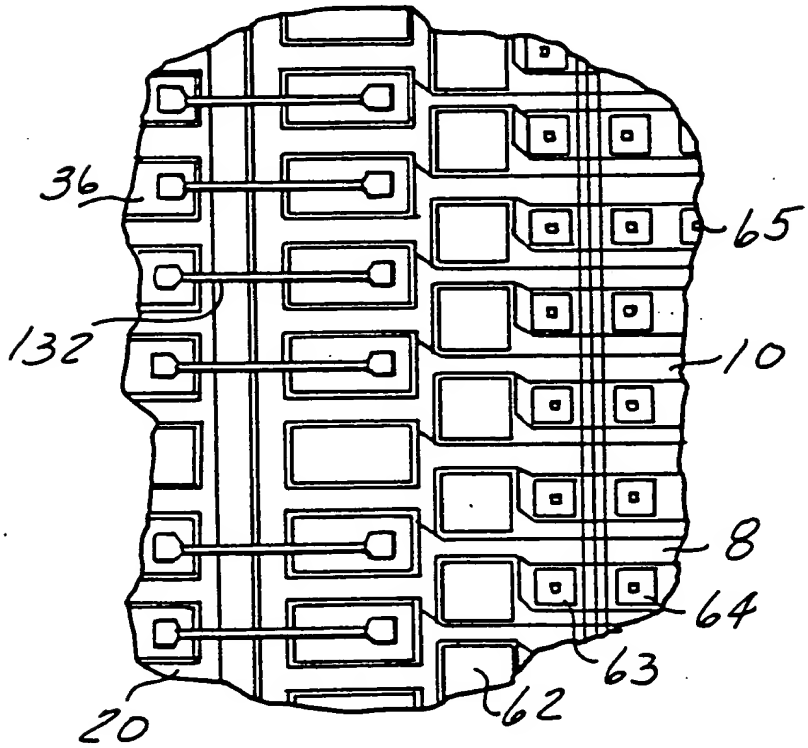

FIG-12

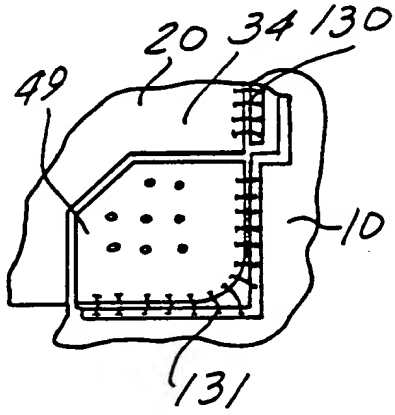

FIG-13

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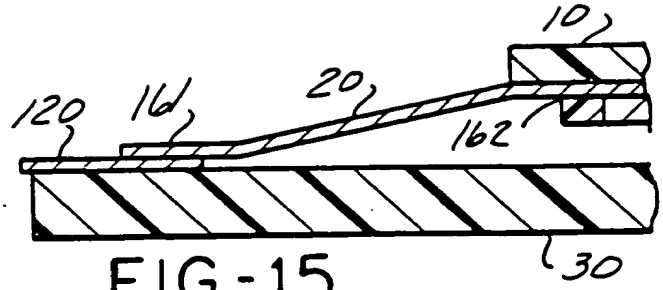

FIG-15

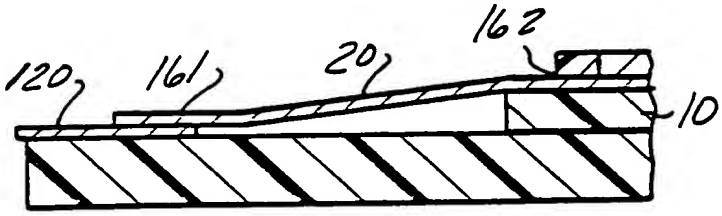

FIG-16

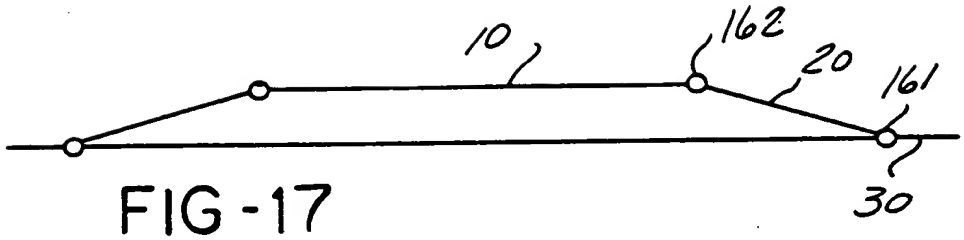

FIG-17

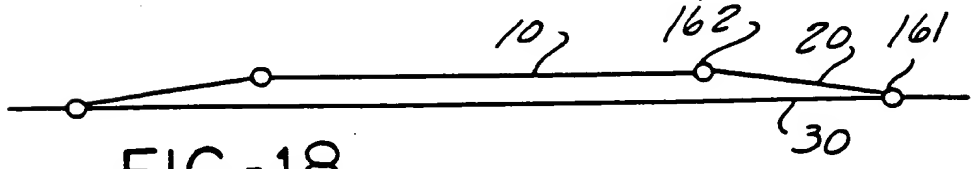

FIG-18

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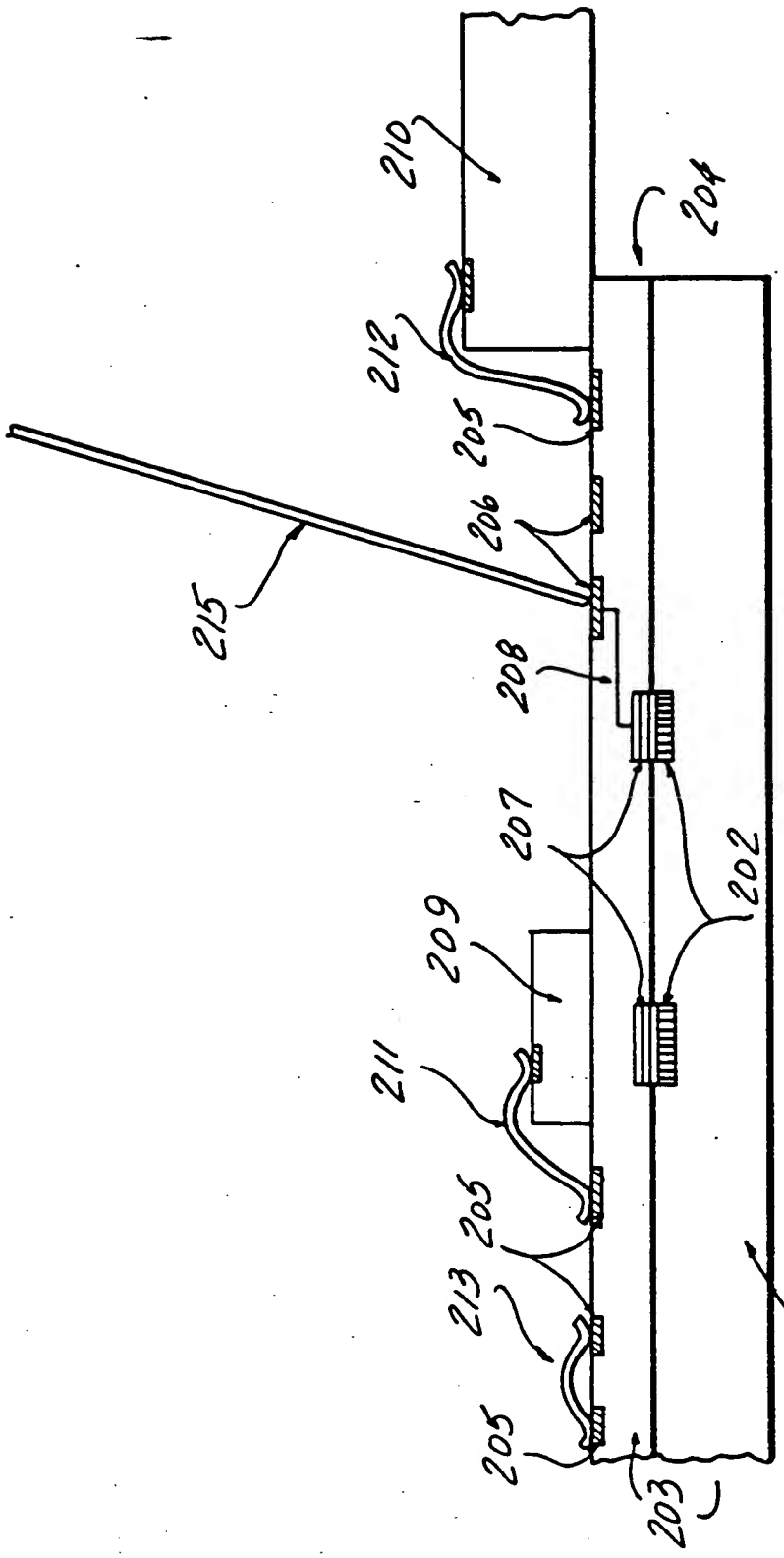

FIG-19

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